OpenFPGA:
A Complete Open Source Framework for FPGA Prototyping

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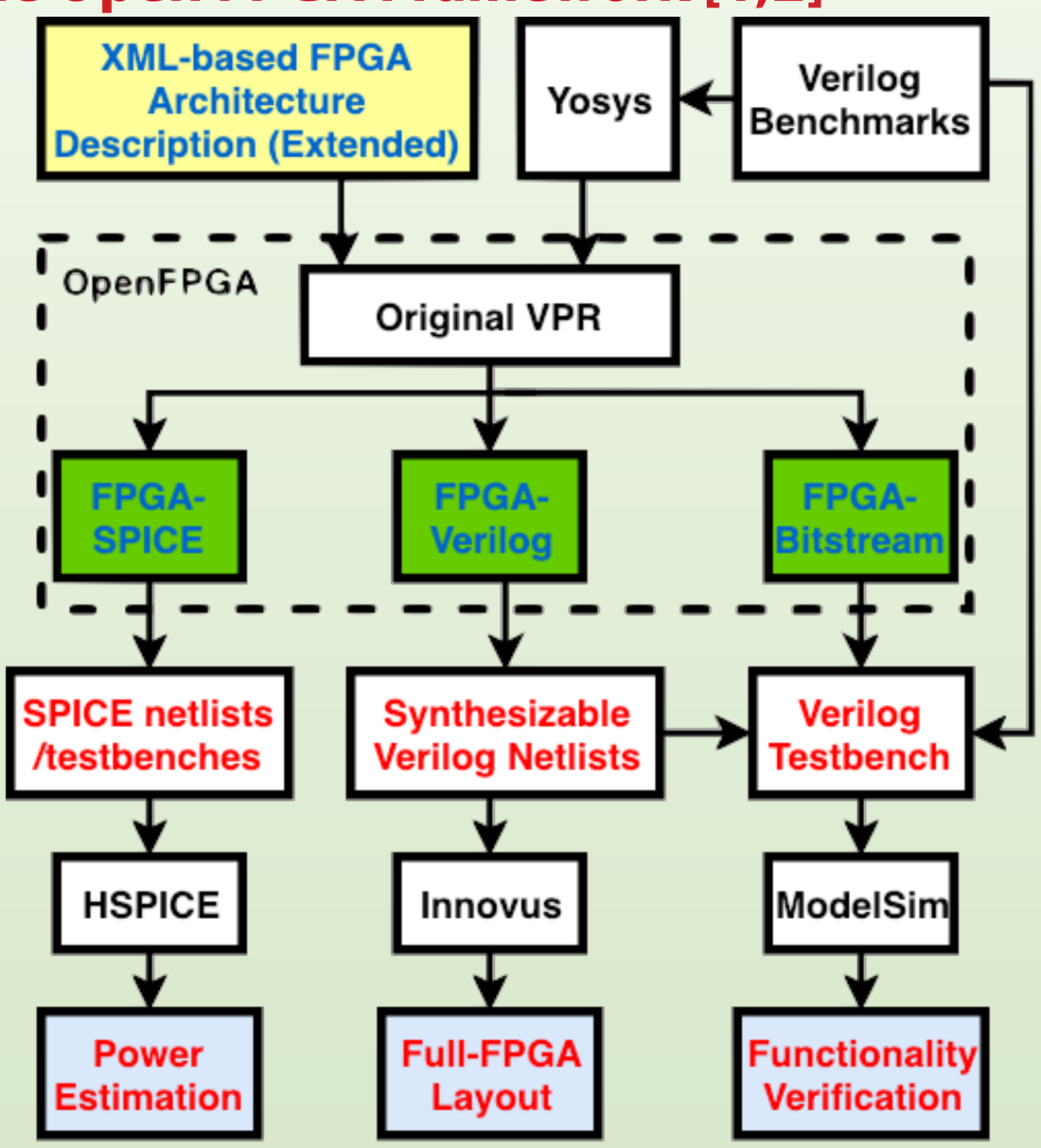
Introduction

* **FPGA** exploration needs more precise and realistic timing analysis, area estimation and power consumption.
* Customizable fabrics show lots of promise for **emerging applications**
* We propose the first **Open Source framework** allowing **production ready** configurable fabrics with **high customizability**

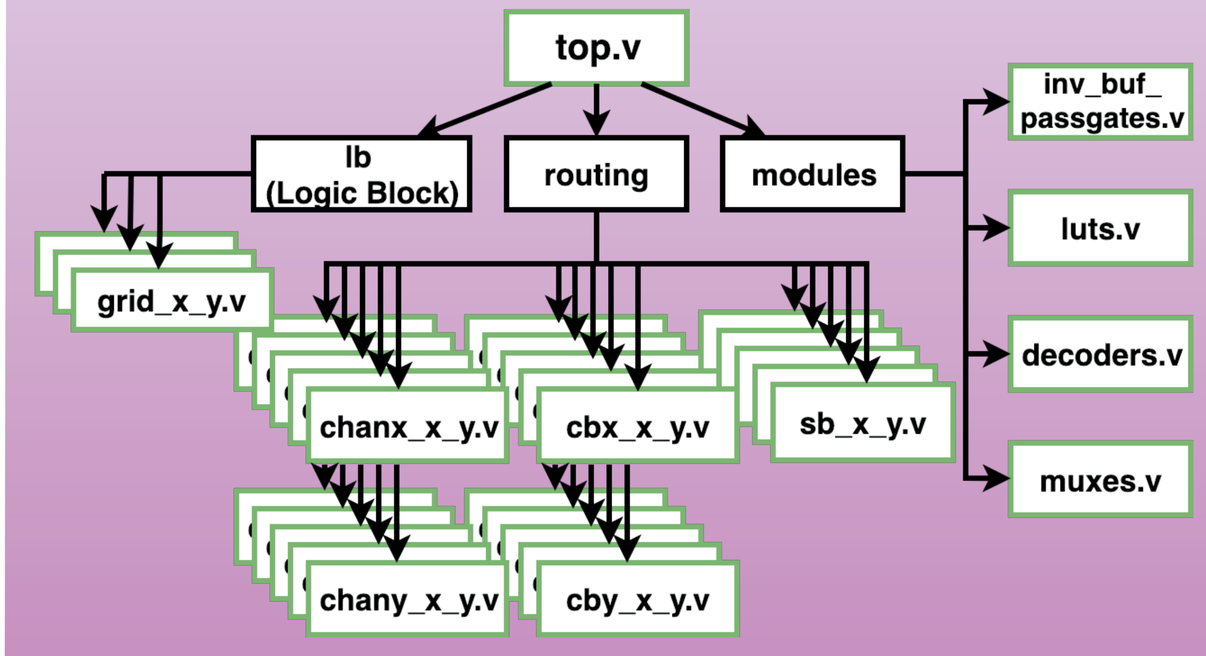
The Open FPGA Framework [1,2]



Complete framework proposed in this work

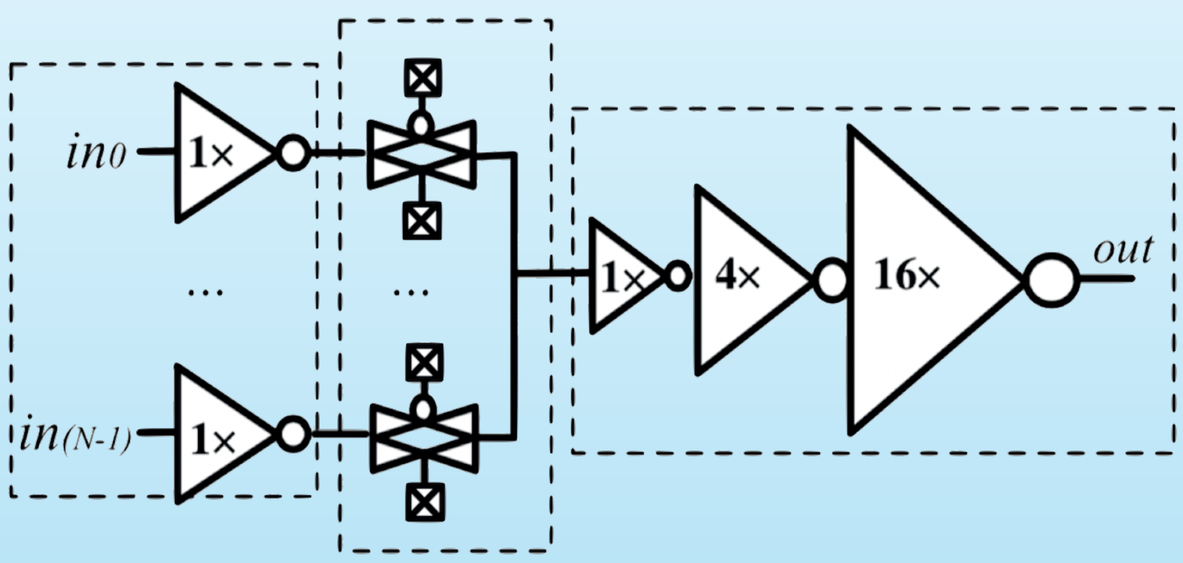
- **XML** architecture extension
- Integration of **Yosys**
- 3 outputs, **SPICE**, **Verilog** and **Bitstream** for:
  - Golden standard simulations
  - Hierarchical Verilog output
  - Bitstream generation for benchmarks

Generation of a hierarchical, synthesizable Verilog



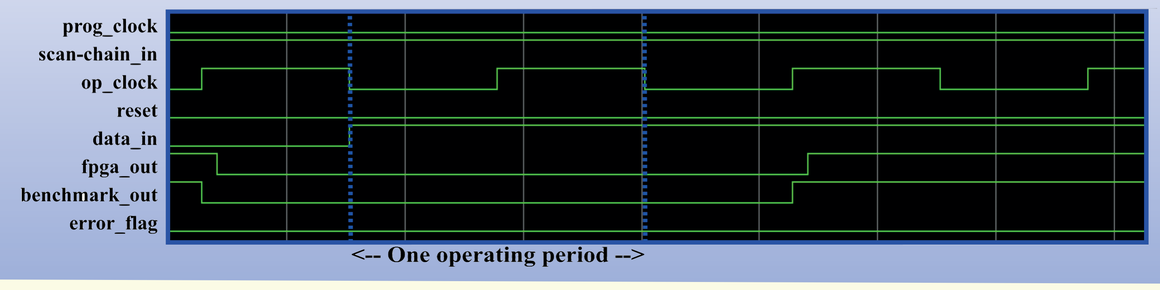
Fully-hierarchical generation for easier implementation

Circuit-level Implementation Support



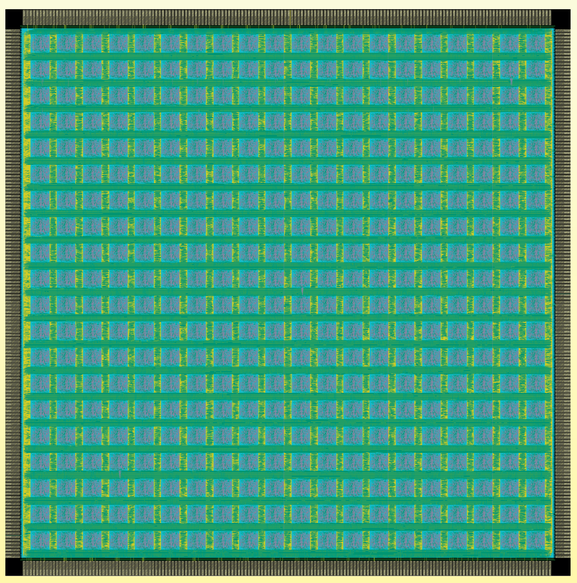
- Automatic generation of buffers, even multi level
- Choice of **Mux**, **1-level**, **2-level** or **tree-like**
- Auto-generated **Inverters**, **pass-transistor/transmission-gate**, **LUTs**
- Integration of **Hard Logic**
- **I/O Pads**

Functional Verification



Place and Route of a generated 20x20 FPGA Fabric

- Semi-custom design tool:
  CADENCE Innovus
- **FPGA** characteristics:
  - **N = 10**
  - **k = 6**
  - Area: **10.3 mm²**



Conclusion

- Integration of flexible elements such as **MUXs, transmission-gates or LUTs**
- Generation of the **Verilog** of an **homogeneous FPGA 20x20** ready to be taped-out
- **Functional verification** assuring that the functionnality is correct

Open Source Design Automation (OSDA) 2019

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References: [1] https://github.com/LNIS-Projects/OpenFPGA
[2] https://openfpga.readthedocs.io/en/master/

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